ALPHA DATA

ADM-XRC-5T1 User Manual

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1 Introduction

The ADM-XRC-5T1 is a high performance PCI Mezzanine Card (PMC) designed for applications using the Virtex™-5 FPGAs from Xilinx. This card supports VIrtex-5 LX110T, LX155T, SX95T and FX70T devices with the FFG1136 package.

The card uses an FPGA PCI bridge developed by Alpha-Data supporting PCI-X and PCI. This allows high performance PCI-X / PCI operation without the need to integrate proprietary cores into the FPGA.

A high-speed multiplexed address/data bus connects the bridge to the target (user) FPGA.

The card can also be fitted with a Primary XMC connector to provide high-speed serial link connections to the user FPGA.

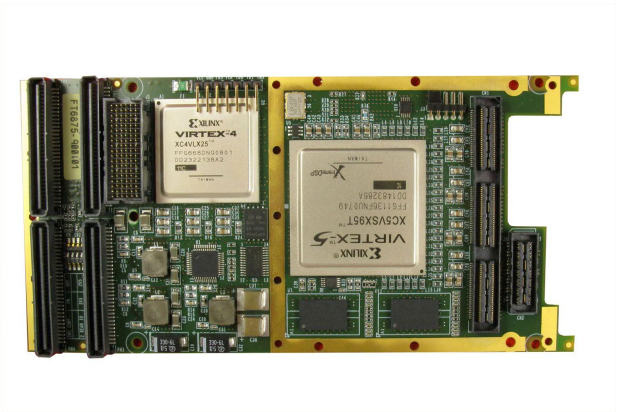

Figure 1: ADM-XRC-5T1

1.1 Specifications

The ADM-XRC-5T1 supports high performance PCI-X / PCI operation without the need to integrate proprietary cores into the FPGA.

- Physically conformant to VITA 42 XMC Standard
- Physically conformant to IEEE P1386-2001 Common Mezzanine Card standard (with XMC connector removed)
- 8-lane PCIe / Serial RapidIO connections to User FPGA (via XMC connector)
- 8 additional MGT links to User FPGA. (via front-panel adaptor)
- High performance PCI and DMA controllers
- Local bus speeds of up to 80 MHz
- Two independent banks of 64Mx32 DDRII SDRAM (512MB total)
- One bank of 2Mx18 DDRII SSRAM (4MB total)
- User clock programmable between 31.25MHz and 625MHz
- Stable low-jitter 200MHz clock for precision IO delays
- User front panel adapter with up to 146 free IO signals
- User rear panel PMC connector with 64 free IO signals
- Programmable I/O voltage on front and rear interfaces
- Supports 3.3V PCI or PCI-X at 64 bits

2 Hardware Installation

This chapter explains how to install the ADM-XRC-5T1 onto a PMC motherboard or carrier.

2.1 Handling instructions

Observe SSD precautions when handling the cards to prevent damage to components by electrostatic discharge.

Avoid flexing the board.

2.1.1 Handling Instructions

The components on this board can be damaged by electrostatic discharge (ESD). To prevent damage, observe SSD precautions:

- Always wear a wrist-strap when handling the card
- Hold the board by the edges
- Avoid touching any components
- Store in ESD safe bag.

2.2 Motherboard / Carrier requirements

The ADM-XRC-5T1 is a 3.3V only PCI device and is not compatible with systems that use 5V signalling.

The ADM-XRC-5T1 must be installed in a PMC motherboard or carrier that supplies +5.0V and +3.3V power to the PMC connectors. Ensure that this requirement is satisfied before powering it up. +12V and -12V may also be required for certain XRM modules.

The current requirements on each power rail are highly dependent on the user FPGA application. A power estimator spreadsheet is available on request from Alpha Data. This should be used in conjunction with Xilinx power estimation tools to determine the exact requirements for each power rail.

2.3 PCI Mode selection

The ADM-XRC-5T1 automatically detects whether the board is connected to a PCI or PCI-X bus.

2.4 Installing the ADM-XRC-5T1 onto a PMC motherboard

Note: This operation should not be performed while the PMC motherboard is powered up.

The ADM-XRC-5T1 must be secured to the PMC motherboard using M2.5 screws in the four holes provided. The PMC bezel through which the I/O connector protrudes should be flush with the front panel of the PMC motherboard.

2.5 Installing the ADM-XRC-5T1 if fitted to an ADC-PMC

The ADM-XRC-5T1 can be supplied for use in standard PC systems fitted to an ADC-PMC carrier board. The ADC-PMC can support up to two PMC cards whilst maintaining host PC PCI compatibility. If you are using a ADC-PMC, refer to the supplied documentation for information on jumper settings. All that is required for installation is a PCI slot that has enough space to accommodate the full-length card. The ADC-PMC is compatible with 5V and 3V PCI (32 and 64 bit) and PCI-X slots.

It should be noted that the ADC-PMC uses a standard bridge to provide a secondary PCI bus for the ADM-XRC-5T1 and that some older BIOS code does not set up these devices correctly. Please ensure you have the latest version of BIOS appropriate for your machine.

2.6 Cooling Requirements

The power consumption of the ADM-XRC-5T1 is highly dependent on the user FPGA application. With large FPGA applications, it is possible that the board may dissipate more than 15W. Although the board is designed to handle this, the user must ensure that it is adequately cooled.

To prevent damage through over-heating, an on-board system monitor will automatically reconfigure the User FPGA with a low-power bitstream if the FPGA reaches 85C or if the board reaches 70C. (100C and 85C respectively for Industrial grade devices).

The FPGA temperature may be measured using a software application or with Xilinx Chipscope and a JTAG cable.

See Section 4.3 for further details of the on-board system monitor.

3 Software Installation

Please refer to the SDK installation CD. The SDK contains drivers, examples for host control and FPGA design and comprehensive help on application interfacing.

4 Board Description

The ADM-XRC-5T1 follows the architecture of the ADM-XRC series and decouples the "target" FPGA from the PCI interface, allowing user applications to be designed with minimum effort and without the complexity of PCI design.

A separate Bridge / Control FPGA interfaces to the PCI bus and provides a simpler Local Bus interface to the target FPGA. It also performs all of the board control functions including the configuration of the target FPGA, programmable clock setup and the monitoring of on-board voltage and temperature.

DDR2 SDRAM, DDR2 SSRAM and serial flash memory connect to the target FPGA. These are supported by Alpha Data or Xilinx IP.

IO functionality is provided using XRM modules. MGT links are connected through a SAMTEC QSE-DP connector, CN2. Remaining signals are connected through a 180 pin SAMTEC QSH connector, CN1.

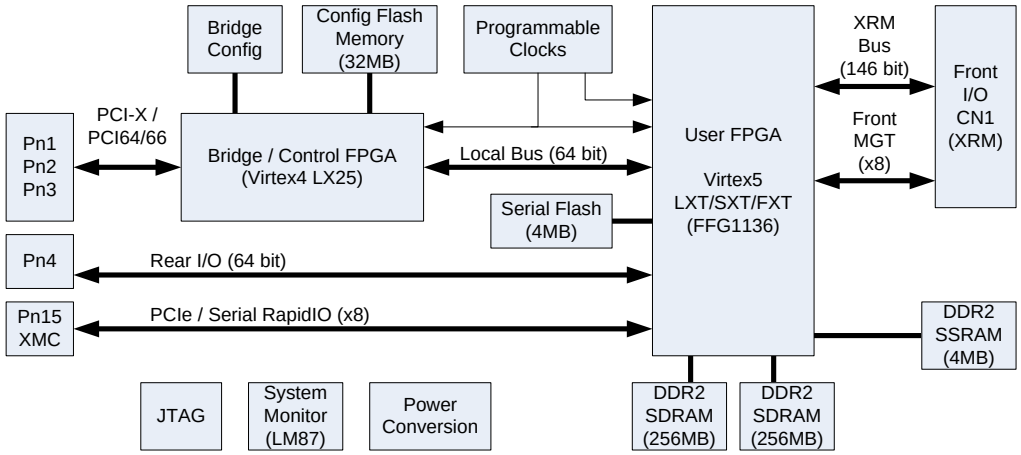

Figure 2: ADM-XRC 5T1 Block Diagram

4.1 Switch Definitions

There is a set of four DIP switches placed between PMC connectors Pn2 & Pn4. Their functions are described in **Table 1, "Switch Definitions"**.

Switch Ref.	Function	ON State	Off State
SW2-1	*Reserved*	-	-
SW2-2	*Rear Voltage Select*	RearIO = 3.3V	RearIO = 2.5V
SW2-3	One-time Configuration	Target FPGA is cleared then configured from Flash at power-up only.	Target FPGA is cleared then configured from flash at power-up and after every board reset (PCI_RST#).
SW2-4	PCI Default	Load Bridge in PCI mode first	Load Bridge in PCI-X mode first (Rev 4 PCB only)

Table 1: Switch Definitions

4.2 Local Bus

The ADM-XRC-5T1 implements a multi-master local bus between the bridge and the target FPGA using a 32- or 64-bit multiplexed address / data path. The bridge design is asynchronous and allows the local bus to be run faster or slower than the PCI bus clock to suit the requirements of the user design.

The local bus runs at 40MHz by default but this can be altered to different frequencies between 32MHz and 80MHz.

Full details of the local bus operation, including timing constraints, DMA and Interrupts are given in the Software Development Kit (SDK).

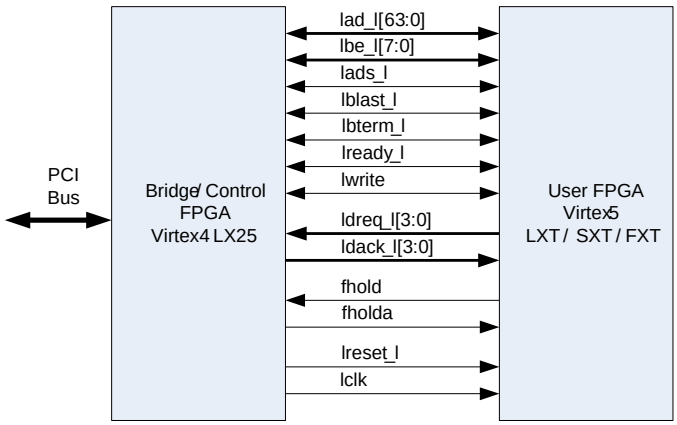

Figure 3: Local Bus Interface

Local Bus		
Signal	Type	Purpose
lad[63:0]	bidir	Address and data bus.
lbe_l[7:0]	bidir	Byte qualifiers
Control Signals		
lads_l	bidir	Indicates address phase
lblast_l	bidir	Indicates last word
lbterm_l	bidir	Indicates ready and requests new address phase
lready_l	bidir	Indicates that target accepts or presents new data
lwrite	bidir	Indicates a write transfer from master
ldreq_l[3:0]	unidir	DMA request from target to bridge
ldack_l[3:0]	unidir	DMA acknowledge from bridge to target
fhold	unidir	Target bus request
fholda	unidir	Bridge bus acknowledge
lreset_l	unidir	Reset to target
lclk	unidir	Clock to synchronise bridge and target

Table 2: Local Bus Interface Signal List

4.3 Flash Memory

The ADM-XRC-5T1 is fitted with two separate Flash memories: one connected to the Bridge / Control FPGA and the other to the User FPGA.

4.3.1 Board Control Flash

A 256Mb Flash memory (Intel / Numonyx PC28F256P30) is used for storing Vital Product Data (VPD), programmable clock parameters and configuration bitstreams for the User FPGA.

Access to this flash device is only possible through control logic registers. The flash is not directly mapped onto the local bus. Programming, erasing and verification of the flash are supported by the ADM-XRC SDK and driver. Utilities are provided to load bitstreams into the flash. These also verify the bitstream is compatible with the target FPGA.

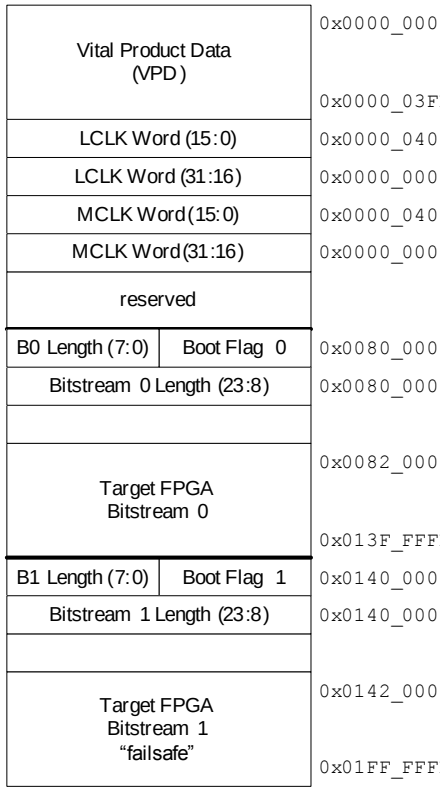

Figure 4: Board Control Flash Organisation

4.3.1.1 Power-Up Sequence

If valid data is stored in the flash memory, the bridge will automatically set the programmable clock generators and configure the User FPGA at power-up.

This sequence can be inhibited by shorting the FBS pin on JTAG connector J2 to GND. See the description of the "FBS" signal in **Section 4.5.2, "FBS"** for further information.

Note: If an over-temperature alert is detected from the System Monitor, the target will be reloaded with the alternate (failsafe) bitstream.

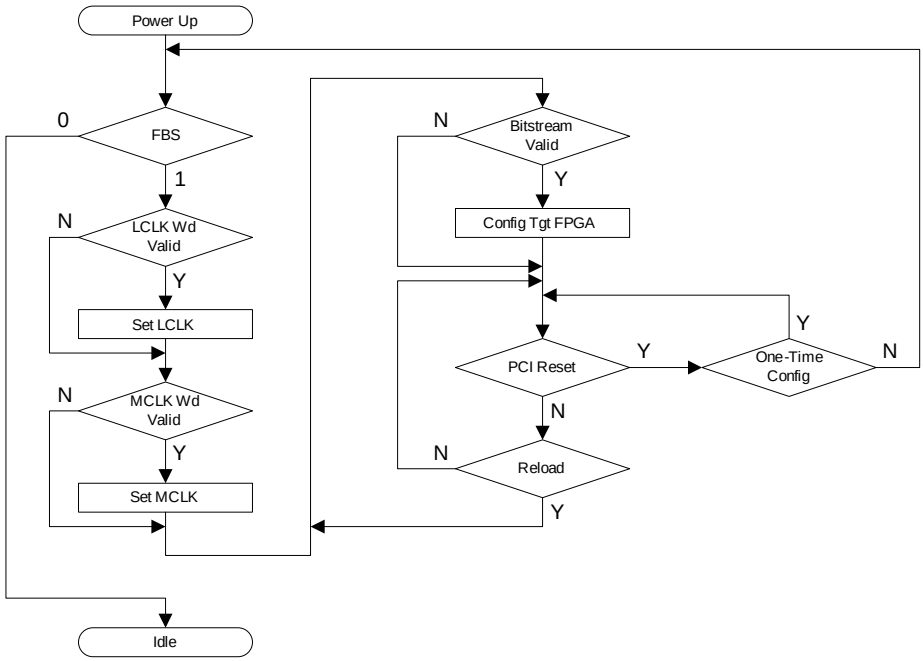

Figure 5: Power-Up Configuration Sequence

4.3.1.2 One-Time Configuration (OTC)

If One-Time Configuration (OTC) is disabled (switch SW2-3 is OFF), the power-up configuration sequence will repeat each time PCI reset is asserted.

If the OTC feature is enabled (switch SW2-3 is ON), the bridge will only set the clocks and configure the User FPGA at power-up. Once the sequence has completed, it will not repeat at PCI reset.

Note: OTC only stops the user FPGA being reconfigured at PCI reset. If does not affect the manual reload function in the bridge control registers, or the over-temperature reload circuit.

4.3.2 User FPGA Flash

An ST M25P32 flash memory with SPI interface is connected to the User FPGA for the storage of application-specific information.

4.4 Health Monitoring

The ADM-XRC-5T1 has the ability to monitor temperature and voltage to maintain a check on the operation of the board. The monitoring is implemented by a National Semiconductor LM87 and is supported by the Bridge FPGA control logic using I2C.

With Bridge FPGA version 3.6 onwards, the LM87 is automatically scanned at approximately once per second. The current voltage and temperature measurements are copied to a blockram within the Bridge FPGA. This allows the values to be read without the need to communicate directly with the LM87.

With Bridge FPGA versions prior to 3.6, voltage and temperature measurements in the LM87 are copied to blockram when instructed by host software.

The following supplies and temperatures, as shown in **Table 3 'Voltage and temperature monitor'**, are monitored.

Monitor	Purpose
1.0V	User FPGA Core Supply
1.2V	Bridge FPGA Core Supply
1.8V	Memories User FPGA Memory I/O Local Bus I/O Config CPLD Core Supply
2.5V	Source voltage for Front Rear I/O
3.3V	Board Input Supply
5.0V	Board Input Supply
Pn4_VCCIO	Either 2.5V or 3.3V Rear (Pn4) I/O Voltage
XRM_VCCIO	Either 2.5V or 3.3V Front Panel I/O Voltage
Temp1	User FPGA die temperature
Temp2	LM87 on die temperature for board/ambient

Table 3: Voltage and temperature monitor

An application is provided in the SDK that permits the reading of the health monitor. The typical output of the monitor is shown below, provided by the SYSMON program.

```
*** SysMon ***
FPGA Space Base Adr = 00900000
Control Space Base Adr = 00d00000
+1V0 Reading = 1.01 V
+1V2 Reading = 1.21 V
+1V8 Reading = 1.81 V
+2V5 Reading = 2.51 V
+3V3 Reading = 3.32 V
+5V Reading = 5.04 V
Pn4 Reading = 3.31 V
FPIO Reading = 3.34 V
SysMon Int Temp = 33 deg. C
User FPGA Temp = 26 deg. C
```

4.4.1 Automatic Temperature Monitoring

At power-up, the control logic sets temperature limits and enables the over-temperature interrupt in the LM87. If the OTC feature is disabled, the limits and interrupt will be re-set after a PCI reset. If OTC is enabled, the limits and interrupt will only be set once at power-up.

The temperature limits are shown in **Table 4 'Temperature Limits'** below:

Environment	User FPGA		Board (LM87 internal)	
	Min	Max	Min	Max
Commercial	0°C	+85°C	0°C	+70°C
Industrial	-40°C	+100°C	-40°C	+85°C

Table 4: Temperature Limits

If any limit is exceeded, the User FPGA is automatically reconfigured with a low-power "failsafe" bitstream.

The purpose of the failsafe mechanism is to protect the card from damage due to overheating. It is possible that the reconfiguration will cause the user application and, possibly, the host computer to hang.

There are three ways to determine if the failsafe bitstream has been loaded:

(1) Data bit (30) in the FPCTL control register will be set.

(2) All local bus reads from the user FPGA will return 0xCAFEFABz, where z = Adr(2).

(3) The device USERCODE (readable using JTAG) = 0x4144DEAD.

Note: With Bridge FPGA version 3.6 onwards, the failsafe mechanism uses an average of the 8 most recent temperature measurements. It also has a 5°C margin outside the limits shown in **Table 4 'Temperature Limits'**. Both measures are to avoid measurement errors causing a false alarm. Bridge FPGA versions prior to 3.6 use only the most recent temperature measurement and have no margin on the limits.

4.5 JTAG

A JTAG header (J2) is provided to allow download of the FPGA using the Xilinx tools and serial download cables. This also allows the use of ChipScope PRO ILA to debug an FPGA design. It should be noted that four devices will be detected when the SCAN chain is initialised.

The JTAG Header pinout is shown in **Figure 6, "JTAG Header J2"**:

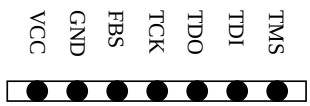

Figure 6: JTAG Header J2

The scan chain is shown in **Figure 7, "JTAG Boundary Scan Chain"**:

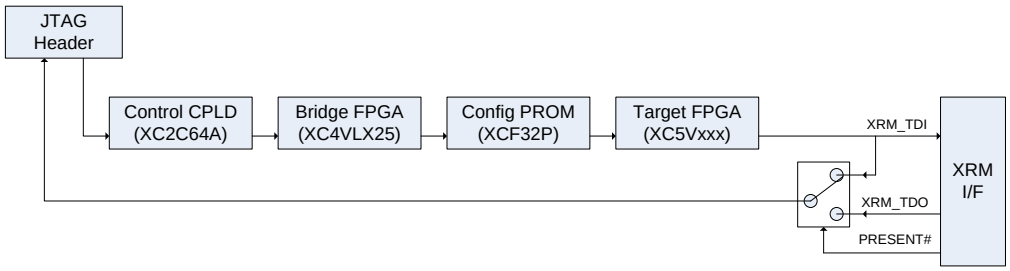

Figure 7: JTAG Boundary Scan Chain

4.5.1 JTAG Voltage

JTAG Vcc = 2.5V and the interface uses 2.5V CMOS signalling. The Vcc supply is protected by a 350mA poly fuse.

4.5.2 FBS

The FBS signal is an input to the control logic and provides control of the cold boot process. By default with no link fitted, the control logic will load a bitstream from flash into the FPGA if one is present. Shorting FBS to the adjacent GND pin will disable this process and can be used to recover situations where rogue bitstreams have been stored in flash.

4.6 Clocks

The ADM-XRC-5T1 is provided with numerous clock sources, as shown in **Figure 8, "Clock Structure"** below:

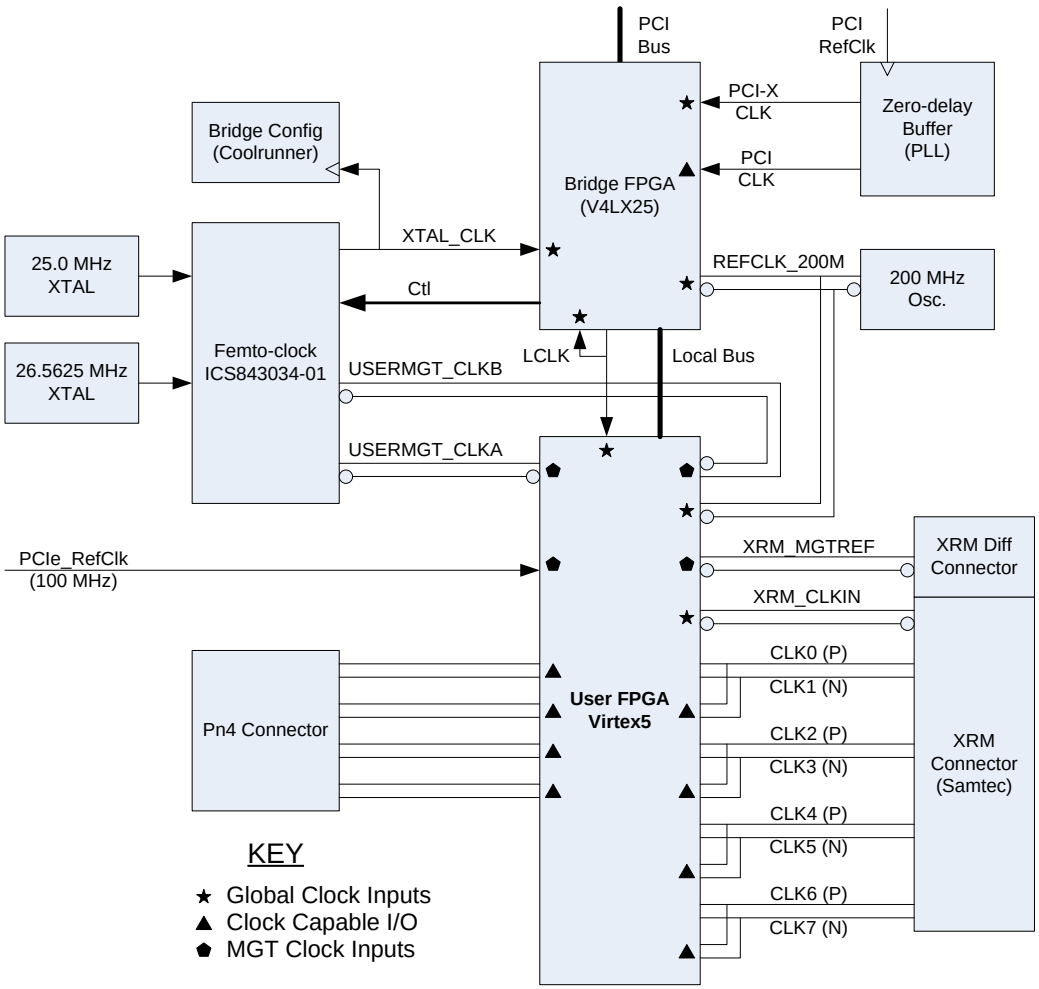

Figure 8: Clock Structure

4.6.1 LCLK

The Local Bus clock, LCLK, is generated from a 200MHz reference by a DCM within the bridge FPGA. The minimum LCLK frequency (determined by the DCM specification) is 32MHz. The maximum is 80MHz.

The LCLK frequency is set by writing DCM multiply & divide values to the LCLOCK register in the bridge. (See SDK for details and example application).

The default LCLK rate is 40MHz and is set on power-up. An alternative default rate can be stored in flash memory:

FlashAdr 0x400 = DCM Multiplier Value - 1

FlashAdr 0x402 = DCM Divider Value - 1

Note: If the user FPGA application includes a DCM driven by LCLK (or one of the other programmable clocks), the clock frequency should be set prior to FPGA configuration.

4.6.2 REFCLK

In order to make use of the IODELAY features of Virtex™-5, a stable low-jitter clock source is required to provide the base timing for tap delay lines in each IOB in the User FPGA. The ADM-XRC-5T1 is fitted with a 200MHz LVPECL (LVDS optional) oscillator connected to global clock resource pins. This reference clock can also be used for application logic if required.

4.6.3 PCIe Reference Clock

A 100MHz PCIe reference clock input from the Primary XMC connector (J1) is connected to one of the dedicated MGT clock inputs on the user FPGA. (See Table 4 for details of the MGT clock connections.)

Note: This clock is not generated on board. It is only available if the carrier provides it and connector J1 is fitted.

4.6.4 User MGT Clocks

A programmable, low-jitter clock source is provided by an ICS843034-01 "FemtoClocks" frequency synthesiser. The synthesiser has two source crystals - one at 26.5625MHz (for Fibre Channel applications) and another at 25.0MHz (suitable for PCIe, Gigabit Ethernet etc.). The synthesiser also has two clock outputs.

"USERMGT_CLKA" is connected to an MGT clock input on the top-half of the user FPGA. It may be used as an alternative to the PCIe reference for the MGTs connected to the Primary XMC.

"USERMGT_CLKB" is connected to an MGT clock input on the bottom half of the user FPGA. It may be used as the reference for the front user MGTs. (See Table 4 for details of the MGT clock connections.)

Note: Either of these clocks can provide a programmable source for applications that do not use MGTs. This requires the instantiation of a GTP_DUAL component within the FPGA. To simplify the task, a wrapper module is provided in the SDK.

The default rate for both USERMGT_CLKA and USERMGT_CLKB is 250MHz and is set on power-up. An alternative default rate can be stored in flash memory:

FlashAdr 0x404 = ClockWord(15:0)

FlashAdr 0x406 = ClockWord(31:16)

See the ICS843034-01 datasheet for details of the programming clock word.

4.6.5 XRM MGT Clock

An XRM module can provide an MGT (GTP) reference clock input for user-specific applications.

Clock Name	GTP No.	FPGA Pin (P/N)	Reference for
PCIE_REFCLK	126	AL7 / AM7	Primary XMC (J1) MGTs
USERMGT_CLKA	122	AL5 / AL4	Primary XMC (J1) MGTs
XRM_MGTREF	120	E4 / D4	Front (CN2) user MGTs
USERMGT_CLKB	112	P4 / P3	Front (CN2) user MGTs

Table 5: MGT Clock Connections

4.6.6 XRM Global Clock Input

The XRM interface provides a differential input to the User FPGA global clocking resources. The default on-board terminations are suitable for an LVDS clock.

4.6.7 XRM Regional Clocks

The XRM interface provides 8 clock lines that can be either be used single-ended or as 4 LVDS differential pairs. These clocks are routed to Clock-Capable inputs on the User FPGA, providing access to its regional clock capabilities.

Each clock pair can be coupled with 16 pairs of XRM bus signals, as shown in **Table 6 'XRM Bus Regional Clocks'** below:

XRM Clocks	FPGA Bank	XRM bus pairs
0 & 1 (Pair 0)	22	1 - 16
2 & 3 (Pair 1)	18	17 - 32
4 & 5 (Pair 2)	20	33 - 48
6 & 7 (Pair 3)	12	49 - 64

Table 6: XRM Bus Regional Clocks

4.6.8 Rear (Pn4) Clocks

Eight pairs of signals from Pn4 are connected to clock-capable inputs that can be used for regional clocking of the remaining Pn4 signals. See Table 12 for details.

4.6.9 PCI Clocks

The PCI Interface within the bridge FPGA requires a regional clock input for 66MHz PCI operation or a global clock input for PCI-X. To comply with the single-load requirement in the PCI specification, a zero-delay clock buffer is used to route the PCI clock to the two different clock inputs.

The clock buffer has a PLL with a minimum input frequency of 24MHz, potentially causing problems in applications that use the PCI 33MHz mode with a slow clock. In this case, the buffer can be bypassed to provide full PCI 33MHz compatibility.

4.7 User FPGA

4.7.1 Configuration

The ADM-XRC-5T1 performs configuration from the host at high speed using SelectMAP. The FPGA may also be configured from flash or by JTAG via header J2.

Download from the host is the fastest way to configure the User FPGA with 8 bit SelectMAP mode enabled. This permits an ideal configuration speed of up to 80MB/s.

The ADM-XRC-5T1 can be configured to boot the User FPGA from flash on power-up if a valid bit-stream is detected in the flash. Booting from flash will also configure the programmable clocks. See **Section 4.3.1.1, "Power-Up Sequence"** .

4.7.2 I/O Bank Voltages

Bank	Voltage	Description
0	2.5V	Configuration I/F
1, 5, 15, 19, 23	1.8V	DDRII DRAM
2	1.8V	SelectMAP I/F
3	3.3V	Clocks,Serial Flash
4, 6	1.5V	DDRII SRAM
11, 13	2.5V or 3.3V	Pn4 Interface
12, 18, 20, 22	1.8V, 2.5V or 3.3V	XRM Interface
17, 21, 25	1.8V	Local Bus

Table 7: User FPGA I/O Bank Voltages

4.7.3 Memory Interfaces

4.7.3.1 DDRII SDRAM

The ADM-XRC-5T1 has two independent banks of DDRII SDRAM.

Each bank consists of two memory devices in parallel to provide a 32 bit datapath. 1Gb Micron MT47H64M16-3 devices are fitted as standard to provide 256MB per bank. The board supports 2Gb devices and these are available as an ordering option.

Full details of the interface, signalling standards and an example design are provided in the SDK.

4.7.3.2 DDRII SSRAM

The ADM-XRC-5T1 has a single bank of DDRII SSRAM.

The bank consists of a single device to provide a 18 bit datapath. 36Mb GSI8342T18-333 devices are fitted as standard to provide 4MB per bank. The board supports 72Mb devices and these are available as an ordering option.

Full details of the interface, signalling standards and an example design are provided in the SDK.

4.8 XRM Bus and Front Panel I/O

A major benefit of the ADM-XRC series of boards that use the XRM Bus interface is the versatility of I/O options that result. The ADM-XRC-5T2 maintains this interface and thus compatibility with a wide range of I/O modules to suit many diverse needs.

Standard signals and power on the XRM interface use the 180 pin Samtec QSH series connector, CN1. MGT links use the 28 pin Samtec QSE-DP connector, CN2.

4.8.1 XRM Signalling Voltage

The signalling voltage on the XRM connector (and User FPGA Banks 12, 18, 20 & 22) is selectable by jumper J3.

J3	XRM I/O voltage
Link p1 & p2	3.3V
Link p2 & p3	2.5V
Link p3 & p4	2.5V
Link p5 & p4	1.8V

Table 8: XRM I/O Voltage Selection

4.8.2 XRM Interface - Standard Signals and Power

The XRM interface is implemented on CN1, a 180 pin Samtec connector type QSH, with the pin-out as detailed in tables **Table 9 'XRM Interface - part 1'** to **Table 11 'XRM Interface - part 3'**.

The signals that connect to CN1 are provided in the main from four banks of the User FPGA, Banks 12, 18, 20 & 22. These banks share a common VCCO that can be 1.8V, 2.5V or 3.3V powered, selectable with a jumper link on J3.

Note: Signals S_9 and S_10 are connected to a 3.3V FPGA Bank 3 through 100Ω current limiting resistors.

Signal	FPGA Pin	Samtec Pin	Samtec Pin	FPGA Pin	Signal
N_1	AP14	1	2	AA10	N_2
P_1	AN14	3	4	AB10	P_2
N_3	AM13	5	6	AA8	P_4
P_3	AN13	7	8	AA9	N_4
N_5	AB8	9	10	AM11	N_6
P_5	AC8	11	12	AM12	P_6
N_7	AC9	13	14	AL10	N_8
P_7	AC10	15	16	AL11	P_8
P_9	AE8	17	18	AK11	P_10
N_9	AD9	19	20	AJ11	N_10
N_11	AK9	21	22	AJ10	N_12
P_11	AK8	23	24	AJ9	P_12
N_13	AE11	25	26	AH9	P_14
P_13	AF11	27	28	AH10	N_14
N_15	AH8	29	30	AG10	P_16
P_15	AG8	31	32	AG11	N_16
N_17	AC5	33	34	AB7	N_18
P_17	AC4	35	36	AB6	P_18
S_1	AP12	37	38	AD10	CLK0
+3.3V		39	40	AD11	CLK1
+3.3V		41	42		XRM_SERID
+3.3V		43	44		RESERVED
+5V		45	46		XRM_VREF
+5V		47	48		XRM_VCCIO
VBAT		49	50		XRM_VCCIO
+12V		51	52		XRM_VCCIO
+12V		53	54		-12V
PRESENCE_L		55	56		XRM_TDI
XRM_TCK		57	58		XRM_TRST
XRM_TMS		59	60		XRM_TDO

Table 9: XRM Interface - part 1

Signal	FPGA Pin	Samtec Pin	Samtec Pin	FPGA Pin	Signal
N_19	AB5	61	62	AD7	N_20
P_19	AA5	63	64	AC7	P_20
N_21	AD5	65	66	Y7	N_22
P_21	AD4	67	68	AA6	P_22
N_23	AE6	69	70	Y6	N_24
P_23	AD6	71	72	W6	P_24
N_25	AF6	73	74	W7	P_26
P_25	AE7	75	76	V7	N_26
P_27	Y11	77	78	W9	N_28
N_27	W11	79	80	W10	P_28
N_29	AJ6	81	82	V8	P_30
P_29	AJ7	83	84	U8	N_30
N_31	AK6	85	86	V9	N_32
P_31	AK7	87	88	V10	P_32
CLK2	AG5	89	90	AH7	S_4
CLK3	AF5	91	92	D11	S_5
S_2	AF9	93	94	M8	S_6
S_3	Y8	95	96	L4	S_7
CLK4	K8	97	98	F8	N_34
CLK5	K9	99	100	F9	P_34
N_33	E8	101	102	T8	CLK6
P_33	E9	103	104	U7	CLK7
S_8	R11	105	106	H20	S_10
S_9	H19	107	108	H15	XRM_CLKIN_N
XRM_MGTREF_P	E4	109	110	H14	XRM_CLKIN_P
XRM_MGTREF_N	D4	111	112	H13	XRM_SDA
XRM_PECL_N	J21	113	114	J14	XRM_SCL
XRM_PECL_P	J20	115	116		RESERVED
XRM_TX7_P	B10	117	118	A9	XRM_RX7_P
XRM_TX7_N	B9	119	120	A8	XRM_RX7_N

Table 10: XRM Interface - part 2

Signal	FPGA Pin	Samtec Pin	Samtec Pin	FPGA Pin	Signal
P_35	F10	121	122	G8	P_36
N_35	G10	123	124	H8	N_36
N_37	J11	125	126	D12	P_38
P_37	K11	127	128	C12	N_38
P_39	H10	129	130	A13	P_40
N_39	H9	131	132	B12	N_40
N_41	J9	133	134	C13	N_42
P_41	J10	135	136	B13	P_42
P_43	G11	137	138	E11	N_44
N_43	G12	139	140	F11	P_44
P_45	M10	141	142	E13	N_46
N_45	L9	143	144	E12	P_46
N_47	N9	145	146	N8	P_50
P_47	N10	147	148	N7	N_50
P_49	M6	149	150	G13	N_48
N_49	M5	151	152	F13	P_48
P_51	M7	153	154	P5	N_52
N_51	L6	155	156	N5	P_52
N_53	P6	157	158	K6	N_54
P_53	P7	159	160	K7	P_54
P_55	R6	161	162	J5	N_56
N_55	T6	163	164	J6	P_56
N_57	R8	165	166	J7	N_58
P_57	R7	167	168	H7	P_58
N_59	G5	169	170	F6	N_60
P_59	H5	171	172	F5	P_60
N_61	T11	173	174	G7	N_62
P_61	T10	175	176	G6	P_62
N_63	U10	177	178	E7	N_64
P_63	T9	179	180	E6	P_64

Table 11: XRM Interface - part 3

4.8.3 XRM Interface - MGT Links

Eight lanes of user MGT (GTP) links are routed to the XRM interface. Lanes 0 - 6 are routed through Samtec QSE-DP connector, CN2. Lane 7 is routed through the Samtec QSH connector, CN1.

Signal	FPGA Pin	GTP Number	Samtec Pin
XRM_TX0_P	U2	112B	1
XRM_TX0_N	T2		3
XRM_RX0_P	T1		2
XRM_RX0_N	R1		4
XRM_TX1_P	M2	112A	5
XRM_TX1_N	N2		7
XRM_RX1_P	N1		6
XRM_RX1_N	P1		8
XRM_TX2_P	L2	116B	17
XRM_TX2_N	K2		19
XRM_RX2_P	K1		18
XRM_RX2_N	J1		20
XRM_TX3_P	F2	116A	21
XRM_TX3_N	G2		23
XRM_RX3_P	G1		22
XRM_RX3_N	H1		24
XRM_TX4_P	E2	120B	9
XRM_TX4_N	D2		11
XRM_RX4_P	D1		10
XRM_RX4_N	C1		12
XRM_TX5_P	B4	120A	13
XRM_TX5_N	B3		15
XRM_RX5_P	A3		14
XRM_RX5_N	A2		16
XRM_TX6_P	B5	124B	25
XRM_TX6_N	B6		27
XRM_RX6_P	A6		26
XRM_RX6_N	A7		28
XRM_TX7_P	B10	124A	(CN1) 117
XRM_TX7_N	B9		(CN1) 119
XRM_RX7_P	A9		(CN1) 118
XRM_RX7_N	A8		(CN1) 120

Table 12: XRM Interface - MGT Links

4.9 Pn4 I/O

Up to 32 pairs of differential or 64 single-ended signals are available on Pn4 and are sourced from Banks 11 and 13 of the User FPGA. All of the signal traces are routed as 100Ω differential pairs and each pair is matched in length. The worst case difference in trace length between any two pairs is 10mm.

Signal	FPGA Pin	Pn4 Pin	Pn4 Pin	FPGA Pin	Signal
PN4_P1	AN34	1	2	AM33	PN4_P2
PN4_N1	AN33	3	4	AM32	PN4_N2
PN4_P3	AL34	5	6	AJ32	PN4_P4
PN4_N3	AL33	7	8	AK32	PN4_N4
PN4_P5	AK34	9	10 [CC]	AD32	PN4_P6
PN4_N5	AK33	11	12 [CC]	AE32	PN4_N6
PN4_P7	AH34 [CC]	13	14 [CC]	AF34	PN4_P8
PN4_N7	AJ34 [CC]	15	16 [CC]	AE34	PN4_N8
PN4_P9	AF33 [CC]	17	18	AC33	PN4_P10
PN4_N9	AE33 [CC]	19	20	AB33	PN4_N10
PN4_P11	AC32	21	22	AC34	PN4_P12
PN4_N11	AB32	23	24	AD34	PN4_N12
PN4_P13	AA34	25	26	Y33	PN4_P14
PN4_N13	Y34	27	28	AA33	PN4_N14
PN4_P15	W34	29	30	V32	PN4_P16
PN4_N15	V34	31	32	V33	PN4_N16
PN4_P17	U33	33	34	R33	PN4_P18
PN4_N17	T34	35	36	R32	PN4_N18
PN4_P19	T33	37	38	P32	PN4_P20
PN4_N19	R34	39	40	N32	PN4_N20
PN4_P21	L33	41	42	K33 [CC]	PN4_P22
PN4_N21	M32	43	44	K32 [CC]	PN4_N22
PN4_P23	L34 [CC]	45	46	H34 [CC]	PN4_P24
PN4_N23	K34 [CC]	47	48	J34 [CC]	PN4_N24
PN4_P25	J32 [CC]	49	50	G33	PN4_P26
PN4_N25	H33 [CC]	51	52	F34	PN4_N26
PN4_P27	E32	53	54	F33	PN4_P28
PN4_N27	E33	55	56	E34	PN4_N28
PN4_P29	C34	57	58	C32	PN4_P30
PN4_N29	D34	59	60	D32	PN4_N30
PN4_P31	B33	61	62	B32	PN4_P32
PN4_N31	C33	63	64	A33	PN4_N32

Table 13: Pn4 to FPGA Assignments

In **Table 13 'Pn4 to FPGA Assignments'**, pins marked [CC] are clock capable and may be used to access the regional clocking resources in the FPGA.

Banks 11 & 13 are fitted with resistors to allow DCI terminations on Pn4 signals.

4.9.1 Pn4 Signalling Voltage

The signalling voltage on the Pn4 connector (and User FPGA Banks 11 & 13) is selectable by switch SW2-2.

Switch Ref.	Function	ON State	Off State
SW2-2	*Rear Voltage Select*	RearIO = 3.3V	RearIO = 2.5V

Table 14: Pn4 I/O Voltage Selection

It should be noted that the switch does not directly route power. The switch position is monitored by the board control logic which, in turn, sets a power multiplexer to use either 2.5V or 3.3V.

4.10 XMC Interface

4.10.1 Primary XMC Connector

The MGT (GTP) links connected between the user FPGA and the Primary XMC connector are compatible with PCI Express and Serial RapidIO. Depending upon the carrier card, they may also be used for user-specific applications.

Note: The Primary XMC connector is defined in the VITA Standard as "P15" but is incorrectly marked as "J1" on the ADM-XRC-5T2. All references to J1 in this document are for the connector in the standard position P15.

Signal	FPGA Pin	GTP Number	P15 Pin
PCIE_TX0_P	AN5	126A	A1
PCIE_TX0_N	AN6		B1
PCIE_RX0_P	AP6		A11
PCIE_RX0_N	AP7		B11
PCIE_TX1_P	AN10	126B	D1
PCIE_TX1_N	AN9		E1
PCIE_RX1_P	AP9		D11
PCIE_RX1_N	AP8		E11
PCIE_TX2_P	AK2	122A	A3
PCIE_TX2_N	AL2		B3
PCIE_RX2_P	AL1		A13
PCIE_RX2_N	AM1		B13
PCIE_TX3_P	AN4	122B	D3
PCIE_TX3_N	AN3		E3
PCIE_RX3_P	AP3		D13
PCIE_RX3_N	AP2		E13
PCIE_TX4_P	AD2	118A	A5
PCIE_TX4_N	AE2		B5
PCIE_RX4_P	AE1		A15
PCIE_RX4_N	AF1		B15
PCIE_TX5_P	AJ2	118B	D5
PCIE_TX5_N	AH2		E5
PCIE_RX5_P	AH1		D15
PCIE_RX5_N	AG1		E15
PCIE_TX6_P	V2	114A	A7
PCIE_TX6_N	W2		B7
PCIE_RX6_P	W1		A17
PCIE_RX6_N	Y1		B17
PCIE_TX7_P	AC2	114B	D7
PCIE_TX7_N	AB2		E7
PCIE_RX7_P	AB1		D17
PCIE_RX7_N	AA1		E17

Table 15: XMC J1 Connections

4.11 XRM IO146 Interface

The following tables provide the pin-out of the XRM-IO146 when fitted to an ADM-XRC-5T2. The signal names P_1/ N_1 etc are internal to the ADM-XRC-5T2. The important mapping is between the Mictor pin and the FPGA pin.

Signal	FPGA Pin	Samtec	Mictor Pin	Mictor Pin	Samtec	FPGA Pin	Signal
P_1	AN14	3	1	2	6	AA8	P_4
N_1	AP14	1	3	4	8	AA9	N_4
P_3	AN13	7	5	6	4	AB10	P_2
N_3	AM13	5	7	8	2	AA10	N_2
P_5	AC8	11	9	10	12	AM12	P_6
N_5	AB8	9	11	12	10	AM11	N_6
P_7	AC10	15	13	14	16	AL11	P_8
N_7	AC9	13	15	16	14	AL10	N_8
P_9	AE8	17	17	18	18	AK11	P_10
N_9	AD9	19	19	20	20	AJ11	N_10
P_11	AK8	23	21	22	24	AJ9	P_12
N_11	AK9	21	23	24	22	AJ10	N_12
P_13	AF11	27	25	26	26	AH9	P_14
N_13	AE11	25	27	28	28	AH10	N_14
P_15	AG8	31	29	30	30	AG10	P_16
N_15	AH8	29	31	32	32	AG11	N_16
S_1	AP12	37	33	34	38	AD10	CLK0
S_2	AF9	93	35	36	40	AD11	CLK1
+5V		-	37	38	90	AH7	S_4

Table 16: IO146 Mictor Connector Pins 1 - 38

Signal	FPGA Pin	Samtec	Mictor Pin	Mictor Pin	Samtec	FPGA Pin	Signal
P_17	AC4	35	39	40	36	AB6	P_18
N_17	AC5	33	41	42	34	AB7	N_18
P_19	AA5	63	43	44	64	AC7	P_20
N_19	AB5	61	45	46	62	AD7	N_20
P_21	AD4	67	47	48	68	AA6	P_22
N_21	AD5	65	49	50	66	Y7	N_22
P_23	AD6	71	51	52	72	W6	P_24
N_23	AE6	69	53	54	70	Y6	N_24
P_25	AE7	75	55	56	74	W7	P_26
N_25	AF6	73	57	58	76	V7	N_26
P_27	Y11	77	59	60	80	W10	P_28
N_27	W11	79	61	62	78	W9	N_28
P_29	AJ7	83	63	64	82	V8	P_30
N_29	AJ6	81	65	66	84	U8	N_30

Table 17: IO146 Mictor Connector Pins 39 - 76 (continued on next page)

Signal	FPGA Pin	Samtec	Mictor Pin	Mictor Pin	Samtec	FPGA Pin	Signal
P_31	AK7	87	67	68	88	V10	P_32
N_31	AK6	85	69	70	86	V9	N_32
S_8	R11	105	71	72	89	AG5	CLK2
S_9	H19	107	73	74	91	AF5	CLK3
+5V		-	75	76	95	Y8	S_3

Table 17: IO146 Mictor Connector Pins 39 - 76

Signal	FPGA Pin	Samtec	Mictor Pin	Mictor Pin	Samtec	FPGA Pin	Signal
P_33	E9	103	77	78	100	F9	P_34
N_33	E8	101	79	80	98	F8	N_34
P_35	F10	121	81	82	122	G8	P_36
N_35	G10	123	83	84	124	H8	N_36
P_37	K11	127	85	86	126	D12	P_38
N_37	J11	125	87	88	128	C12	N_38
P_39	H10	129	89	90	130	A13	P_40
N_39	H9	131	91	92	132	B12	N_40
P_41	J10	135	93	94	136	B13	P_42
N_41	J9	133	95	96	134	C13	N_42
P_43	G11	137	97	98	140	F11	P_44
N_43	G12	139	99	100	138	E11	N_44
P_45	M10	141	101	102	144	E12	P_46
N_45	L9	143	103	104	142	E13	N_46
P_47	N10	147	105	106	152	F13	P_48
N_47	N9	145	107	108	150	G13	N_48
S_5	D11	92	109	110	97	K8	CLK4
S_6	M8	94	111	112	99	K9	CLK5
+5V		-	113	114	-		+5V

Table 18: IO146 Mictor Connector Pins 77 - 114

Signal	FPGA Pin	Samtec	Mictor Pin	Mictor Pin	Samtec	FPGA Pin	Signal
P_49	M6	149	115	116	146	N8	P_50
N_49	M5	151	117	118	148	N7	N_50
P_51	M7	153	119	120	156	N5	P_52
N_51	L6	155	121	122	154	P5	N_52
P_53	P7	159	123	124	160	K7	P_54
N_53	P6	157	125	126	158	K6	N_54
P_55	R6	161	127	128	164	J6	P_56
N_55	T6	163	129	130	162	J5	N_56
P_57	R7	167	131	132	168	H7	P_58
N_57	R8	165	133	134	166	J7	N_58

Table 19: IO146 Mictor Connector Pins 115 - 152 (continued on next page)

Signal	FPGA Pin	Samtec	Mictor Pin	Mictor Pin	Samtec	FPGA Pin	Signal
P_59	H5	171	135	136	172	F5	P_60
N_59	G5	169	137	138	170	F6	N_60
P_61	T10	175	139	140	176	G6	P_62
N_61	T11	173	141	142	174	G7	N_62
P_63	T9	179	143	144	180	E6	P_64
N_63	U10	177	145	146	178	E7	N_64
S_7	L4	96	147	148	102	T8	CLK6
S_10	H20	106	149	150	104	U7	CLK7
+5V		-	151	152	-		+5V

Table 19: IO146 Mictor Connector Pins 115 - 152

4.12 XRM HSSDC2A Interface

Signal	FPGA Pin	GTP Number	Samtec Pin	XRM Pin
XRM_TX0_P	U2	102B	CN2-1	P1-6
XRM_TX0_N	T2		CN2-3	P1-5
XRM_TX1_P	M2	102A	CN2-5	P2-6
XRM_TX1_N	N2		CN2-7	P2-5
XRM_TX2_P	L2	103B	CN2-17	P3-6
XRM_TX2_N	K2		CN2-19	P3-5
XRM_TX3_P	F2	103A	CN2-21	P4-6
XRM_TX3_N	G2		CN2-23	P4-5
XRM_RX0_P	T1	102B	CN2-2	P1-2
XRM_RX0_N	R1		CN2-4	P1-3
XRM_RX1_P	N1	102A	CN2-6	P2-2
XRM_RX1_N	P1		CN2-8	P2-3
XRM_RX2_P	K1	103B	CN2-18	P3-2
XRM_RX2_N	J1		CN2-20	P3-3
XRM_RX3_P	G1	103A	CN2-22	P4-2
XRM_RX3_N	H1		CN2-24	P4-3

Table 20: XRM-HSSDC2A-5T2 Pinout

Revision History:

Date	Revision	Nature of Change
08-11-2006	0.1	Initial version
12-03-2007	1.0	First Release
27-08-2007	1.1	Minor Revisions
17-12-2007	1.2	Revised wording of motherboard power requirements.
23-12-2010	2.1	2.2: Added note on power estimation and current requirements, 2.3: New section on PCI mode selection, 2.6: New section on cooling requirements, 4.1: New section on switch definitions, 4.2.1: Added diagram of flash organisation, 4.2.1.1: New section on power-up sequence, 4.2.1.2: New section on One-Time Configuration feature, 4.3.1: New section on Automatic Temperature Monitoring, 4.4: Updated description for Bridge version 3.6 onwards, 4.4.1: New section on JTAG voltage, 4.5: New diagram of JTAG scan chain, 4.5.1: Added note on default LCLK rate, 4.5.3: Note on PCIe Clock availability, 4.5.4: Note on MGT clock defaults, 4.6.3: Revised memory interface description, included SSRAM., 4.7.2: Added note on DCI_CASCADE usage. Other minor updates and corrections.
02-04-2012	2.2	4.9: Corrected bank number for the Pn4 signals.

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